AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-15. (canceled)

16. (currently amended) A method comprising:

~~a cache transmitting an address of a cache block to be evicted from the cache on an interface; and~~

~~in response to the transmitting, reading the cache block from a data memory of the cache for transmission on the interface~~

receiving an address placed on a bus that results in a miss of a cache;

determining which cache entry is to be evicted in response to the miss;

placing an evict address of the cache entry to be evicted onto the bus without accessing the cache entry that is to be evicted, the evict address being generated by the cache onto the bus;

notifying to a controller of the cache that the evict address when received is to be treated as a read request;

receiving the evict address on the bus by the cache;

utilizing the received evict address to access the cache entry that is to be evicted from the cache;

transmitting data in the cache entry onto the bus.

17. (currently amended) The method as recited in claim 16 further comprising ~~transmitting the cache block on the interface~~ placing data from the evicted cache entry into a data buffer prior to transmitting the data onto the bus.

18. (currently amended) The method as recited in claim 16 ~~further comprising:~~

~~detecting a miss of a second address in the cache; and~~

~~selecting the cache block for eviction responsive to the detecting~~ wherein the placing the

evict address onto the bus utilizes a write command from the cache, the write command identifying the evict address as a target for a write operation to the cache, but the notifying to the controller causes the controller to treat the write operation to the target as a read operation to read the data from the cache entry for transmitting onto the bus.

19. (currently amended) The method as recited in claim ~~16 wherein the transmitting is part of a write transaction~~ 18 wherein receiving the address and determining which cache entry is to be evicted is performed in a first clock cycle and placing the evict address of the cache entry to be evicted onto the bus is performed in a second clock cycle.

20. (currently amended) The method as recited in claim ~~16 further comprising storing the cache block in a data buffer responsive to the reading~~ 19 wherein the first and second clock cycles are separated by other clock cycles which have other transactions on the bus.

21. (new) A method comprising:

receiving an address placed on a bus that results in a miss of a cache;

determining which cache block is to be evicted in response to the miss;

placing an evict address of the cache block to be evicted onto the bus if the cache block contains dirty data, the evict address being generated by the cache onto the bus to be received by the cache;

notifying that the evict address when received is to be treated as a read request to the cache;

receiving the evict address on the bus by the cache;

utilizing the received evict address to access the cache block to evict dirty data;

transmitting dirty data onto the bus for data update due to eviction.

22. (new) The method as recited in claim 21 wherein the placing the evict address onto the bus utilizes a write command from the cache, the write command identifying the evict address as a target for a write operation to the cache, but the notifying causes the write operation to the target to be treated as a read operation to read dirty data from the cache clock.

23. (new) The method as recited in claim 22 wherein the placing the evict address includes placing a tag address of the cache block to be evicted as part of the evict address.

24. (new) The method as recited in claim 23 wherein receiving the address and determining which cache block is to be evicted is performed in a first clock cycle and placing and receiving the evict address of the cache block to be evicted onto the bus is performed in a second clock cycle.

25. (new) The method as recited in claim 24 wherein the first and second clock cycles are separated by other clock cycles which have other transactions on the bus.

26. (new) The method as recited in claim 25 further comprising placing the dirty data from the evicted entry into a data buffer prior to transmitting the dirty data onto the bus.

27. (new) The method as recited in claim 21 further comprising queuing the evict address in the cache prior to placing the evict address onto the bus.

28. (new) The method as recited in claim 27 wherein receiving the address and determining which cache block is to be evicted is performed in a first portion of a first clock cycle, queuing the evict address is performed in a second portion of the first clock cycle, placing and receiving the evict address of the cache block to be evicted onto the bus is performed in a first portion of a second clock cycle and reading the dirty data from the cache block is performed in a second portion of the second clock cycle.

29. (new) The method as recited in claim 28 wherein the first and second clock cycles are separated by other clock cycles which have other transactions on the bus.

30. (new) The method as recited in claim 29 further comprising placing the dirty data from the evicted entry into a data buffer prior to transmitting the dirty data onto the bus.